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☐	L28	717/128,129.ccls. and (debug module or debug circuit).ab.	2
☐	L27	717/128,129.ccls. and (debug module or debug circuit or address).ab.	96
☐	L26	L23 and L3	40
☐	L25	L23 and L2	143
☐	L24	L23 and L1	296
☐	L23	L22 or L21 or L20	7946
☐	L22	(714/17 |714/18 |714/30 |714/31 |714/32 |714/33 |714/34 |714/35 |714/36 |714/37 |714/38 |714/39 |714/40 |714/41 |714/42 |714/43).ccls.	5247
☐	L21	(712/32 |712/33 |712/34 |712/35 |712/36).ccls.	1081
☐	L20	(717/124 |717/125 |717/126 |717/127 |717/128 |717/129 |717/130 |717/131 |717/132 |717/133).ccls.	2084
☐	L19	717/124-133.ccls	0
		DB=USPT; PLUR=YES; OP=ADJ	
☐	L18	L11	35
		DB=EPAB,DWPI,TDBD; PLUR=YES; OP=ADJ	
☐	L17	L16	31
		DB=JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=ADJ	
☐	L16	L12 and (information near (trace or debug$))	44
☐	L15	L12 and (bus near (interfac$ or link))	7
☐	L14	L12 and ((bus near communication) same processor)	0
☐	L13	L12 and (bus near (interfac$ or link) same processor)	0
☐	L12	debug$ near (circuit or chip or module)	475
		DB=USPT,PGPB; PLUR=YES; OP=ADJ	
☐	L11	L10 and exception	61
☐	L10	L9 or L8	135
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☐	L8	L1 and ((bus near communication) same processor)	26
☐	L7	L6 and exception	21
☐	L6	L5 or L4	36
☐	L5	L2 and (bus near (interfac$ or link) same processor)	35

☐	L4	L2 and ((bus near communication) same processor)	8
☐	L3	L2 and bus near (interfac$ or link)	73
☐	L2	L1 and information near (trace or debug$)	270
☐	L1	debug$ near (circuit or chip or module)	1127

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File Format: PDF/Adobe Acrobat - View as HTML
Debug module (included on all standard parts except MCF5102) **... Operand Address**. Generation. Operand Fetch 1. Operand Fetch 2. Execute ...
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Instruction address (IA) and **operand address** (OA) watchpoint channels can each match on a range of ... DM: **Debug module** IA: **Instruction address** (watchpoint) ...
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used twice: first, for **operand address** generation and sec- ... Fig.4 ColdFire **debug module** block diagram, showing real-time and background debug datapaths. ...
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> This 32-bit bus connects the core and **debug module** with any on-chip ... The standard execution stage includes an ALU for **operand address** calculations, ...
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SH-5: The 64-Bit SuperH Architecture
... including **instruction address**, instruction code, **operand address**, ... Through an initiator port on the **debug module**, the external debug host can access ...
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EP1089183 St european software patent - Microcomputer debug ...
[0101] A **debug module** 72 containing a debug interface is coupled to system bus 56 via ... For example, if the watchpoint is an **operand address** watchpoint, ...
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There are ten addressing modes six for **operand address**-. ing and four for transfer of control ... COP8 **Debug Module** Moderate cost in-circuit emulation ...
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[PDF] Debug Support on the ColdFire Architecture

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... used twice: first, for **operand address** generation and ... the core asserts cpu_wrt_drc in the **debug module**. ... in the calculation of the target **instruction address**. ...
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[PDF] chitecture
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The on-chip **debug module** contains the debug links and a ... four **instruction-address** range (IA) channels. • two **operand-address** range (OA) channels ...
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